IN THE SPECIFICATION

Please amend the paragraph beginning at page 14, line 15, as follows:

This is conventionally achieved by using a voltage controlled oscillator (VCO) 93, a pre-scaler 113 and a digital frequency synthesiser 115 connected in the manner shown in ~~Figure 5~~ Figure 9. The frequency of the output signal from the VCO 93 is controlled by the input voltage thereto supplied by the synthesiser 115, while the synthesiser receives a version of the VCO output signal, frequency divided by the pre-scaler 113.

Please amend the paragraph beginning at page 14, line 22, and which continues on to page 15, as follows:

Frequency division is conventionally thought of as a digital function and the maximum frequency the pre-scaler 113 can reduce depends on the digital circuit technology used. With RF input signals, bipolar transistor technology is normally used which can operate at the high RF frequencies. However, when a low cost, low power CMOS chip is used for the synthesiser 115 (and perhaps also for the data decoding, processing and control operations of the receiver as a whole), this results in the need for a second chip for performing the frequency division, which increases the cost and size of the transmitter/receiver 90. In contrast, the ~~pre-scaler 103~~ pre-scaler 113 in the transmitter/receiver of Figure 9 uses the novel frequency divider described above. By this feature, every part of the simplex transmitter/receiver 90, with the possible exception of the analog filters, can be built into a single MOS integrated chip, thereby reducing the overall cost and size of the data transmitter/receiver 90. The mixer 107 can be implemented by MOSFET transistors also integrated on the same chip.